R E M A R K S

Careful review and examination of the subject application are noted and appreciated. Applicant's representative thanks Examiner Nguyen for the indication of allowable matter.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 21, 22 and 24 under 35 U.S.C. §112, first paragraph, is respectfully traversed and should be withdrawn.

The subject matter of claims 21, 22 and 24 is fully supported by the drawings and specification as originally filed. As such, the presently pending claims 21, 22 and 24 are fully patentable under 35 U.S.C. §112, first paragraph, and the rejection should be withdrawn. The Office has the burden of presenting evidence or reasoning why a person skilled in the art would not recognize a description of the invention defined by the claims in the Applicant's disclosure (MPEP §2163.04). The description as filed is presumed to be adequate, unless or until sufficient evidence or reasoning to the contrary is presented by the examiner to rebut the presumption (*Id.*).

The conclusory statement in the Office Action that the specification is silent regarding particular claim language does not appear to take into account that claim limitation may be supported in the specification through express, implicit, or

inherent disclosure (MPEP § 2163(I)(B)). Simply because a claim contains words that are different or not present in the specification does not mean the written description is lacking. There is no *in haec verba* requirement (*Id.*).

Contrary to the assertion made in the Office Action, the specification is not silent regarding the cited claim language. Therefore, the Office Action fails to meet the Office's burden to present sufficient evidence or reasoning to rebut the presumption that the description as filed is adequate for a person skilled in the art to recognize a description of the invention defined by the claims in the disclosure (MPEP §2163.04). As such, the rejection of claims 21, 22 and 24 under 35 U.S.C. §112, first paragraph, does not appear to be proper and should be withdrawn.

Specifically, FIGS. 2-5, as originally filed, are block diagrams showing interconnections between a PLD (e.g., element 112, 112', or 112''), a memory (e.g., element 114, 114', or 114'') and a processor (e.g., element 116, 116', or 116''). Block diagrams are commonly used in the electrical arts to convey details about structure and operation of circuits. One skilled in the art would fully recognize that the connections (e.g., lines) between the PLD, the processor and the memory as illustrated in FIGS. 2-5 of the specification can represent interfaces between the respective devices. Therefore, the drawings and specification as filed are adequate for a person skilled in the art to recognize a description

of the invention defined by the claims (MPEP §2163.04). As such, the rejection of claims 21, 22 and 24 under 35 U.S.C. §112, first paragraph, does not appear to be proper and should be withdrawn.

Furthermore, with respect to claim 21, the specification is not silent regarding "an interface configured to couple said programmable logic device with said memory circuit, wherein said programmable logic device is configured by said memory circuit during bootup (as asserted on page 2 of the Office Action)." Specifically, the specification clearly supports the claim language. In particular, the specification recites:

> The configuration data stored in the memory circuit 114 may be used for programming the PLD 112 upon bootup (page 8, lines 5-7 of the specification).

The specification further states:

> Upon bootup, the memory 114′ may be configured to program the PLD 112′ (page 10, lines 3-4, of the specification).

In yet another example of support for the subject matter of claim 21, the specification states:

> Upon a first bootup, the PLD 112″ may be configured as the microprocessor, the micro-controller, the digital signal processor, etc., in response to the instructions stored in the memory 114″ (page 11, lines 9-17 , the specification).

Therefore, the specification would reasonably convey to one skilled in the relevant art that the inventor, at the time that the application was filed, had possession of the claimed invention. As

such, the rejection of claim 21 under 35 U.S.C. §112, first paragraph, does not appear to be proper and should be withdrawn.

With respect to claim 22, the specification would reasonably convey to one skilled in the relevant art that the inventor, at the time that the application was filed, had possession of the claimed invention. Specifically, one skilled in the relevant art would understand, based on the line connecting the processor with the memory in FIGS. 2-4 of the specification, that the processor with the memory could be coupled by an interface. Furthermore, since the line connecting the processor with the memory is labeled "Programs, reads, verifies, erases, etc.," the specification would reasonably convey to one skilled in the relevant art that the processor could perform one or more of programming the memory circuit, reading the memory circuit, verifying the memory circuit and erasing the memory circuit, as presently claimed. As such, the rejection of claim 22 under 35 U.S.C. §112, first paragraph, does not appear to be proper and should be withdrawn.

With respect to claim 24, FIG. 2 of the present specification, as originally filed, would reasonably convey to one skilled in the relevant art, that the inventor, at the time that the application was filed, had possession of the claimed invention. Specifically, one skilled in the relevant art would recognize a first interface configured to couple the programmable logic device

and the memory device in FIG. 2 and the passages cited above in connection with claim 21. One skilled in the art would further recognize that the programmable logic device could be configured by the memory circuit during bootup in light of FIG. 2 and the passages cited above in connection with claim 21. Specifically, FIG. 2 provides a line connecting the memory to the PLD labeled "BOOTUP." One skilled in the art would understand, based on FIG. 2 and the description in the specification, that the line labeled bootup represented the transfer of information from the memory to the PLD during a bootup process.

Furthermore, one skilled in the art would understand that the line connecting the processor 116 in FIG. 2 with the memory 114 in FIG. 2 and labeled "Programs, reads, verifies, erases, etc." can represent a second interface coupling the processor and the memory circuit. Therefore, the specification and drawings as originally filed, would reasonably convey to one skilled in the relevant art that inventor, at the time that the application was filed, had possession of the claimed invention. As such, the rejection of claim 24 under 35 U.S.C §112, first paragraph, does not appear to be proper and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 2, 5, 6, 10-15, 17, 18 and 20 under 35 U.S.C. §103 as being unpatentable over Tang et al. (U.S.

Patent No. 6,389,321; hereinafter Tang) has been obviated by appropriate amendment and should be withdrawn.

The allowable matter of claim 23 has been incorporated into claim 18. Subject matter similar to the allowable matter of claim 23 has been incorporated into claims 1 and 15. Claims 21, 22 and 24 have been amended for consistency with the amendment to claim 18. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.

Robert M. Miller
Registration No. 42,892
24840 Harper Avenue, Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

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